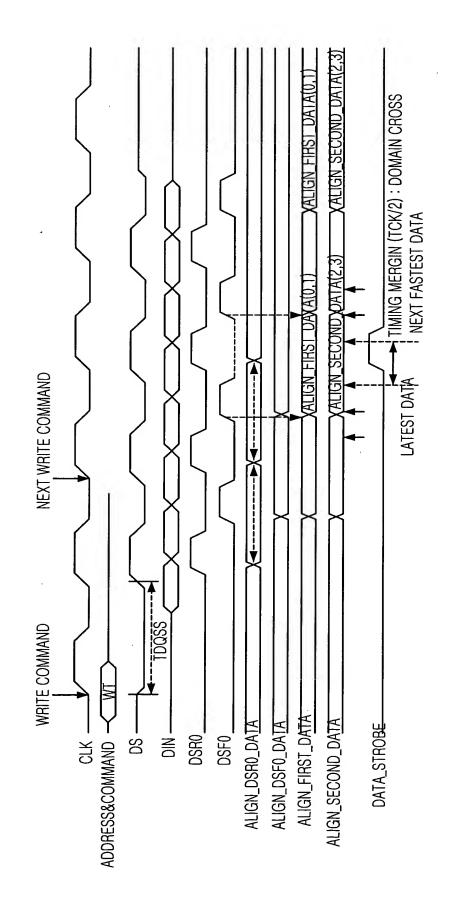
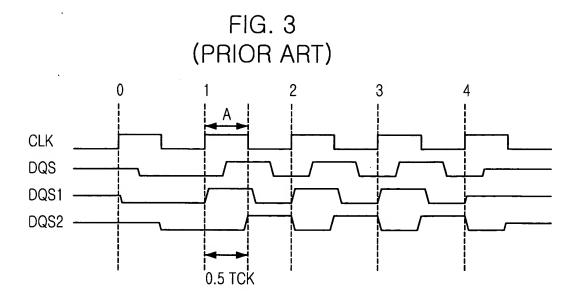
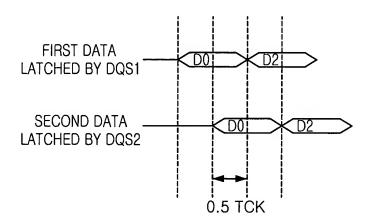
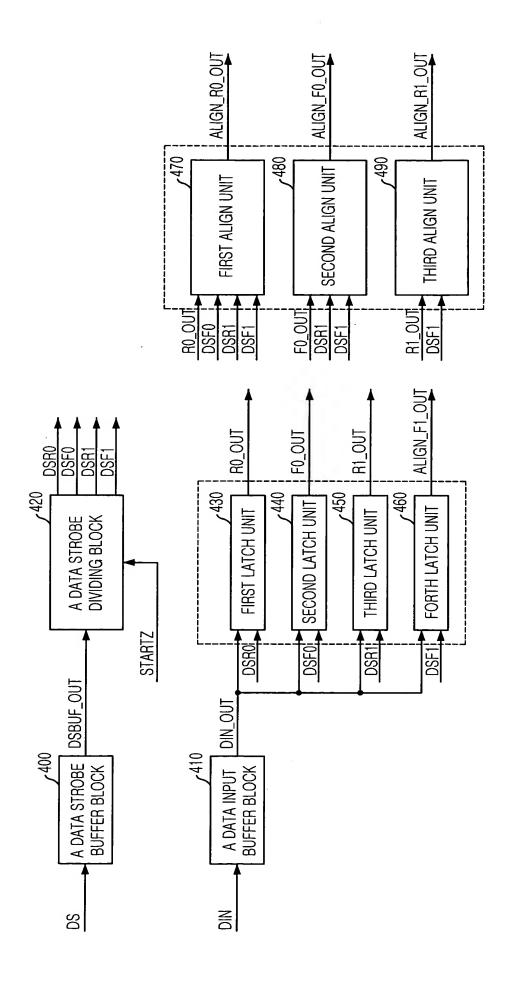
(3)ALIGN\_SECOND\_DATA (2)ALIGN\_SECOND\_DATA (3) AHGN\_SECOND\_DATA (1)ALIGN\_FIRST\_DATA (0)ALIGN\_FIRST\_DATA (1)AHGN\_FIRST\_DATA 150 160 FIRST DATA DIVIDING BLOCK SECOND DATA DIVIDING BLOCK FIG. 1A (PRIOR ART) (PRIOR ART) FIG. 1B ALIGN\_DSR0\_DATA DATA FALLING ALIGN\_DSF0\_DATA INPUT LATCH DSF0 130 DATA RISING INPUT LATCH DS DSFEER DSFO DATA OUTZ ALIGN\_DSR0\_DATA/ALIGN\_DSF0\_DATA

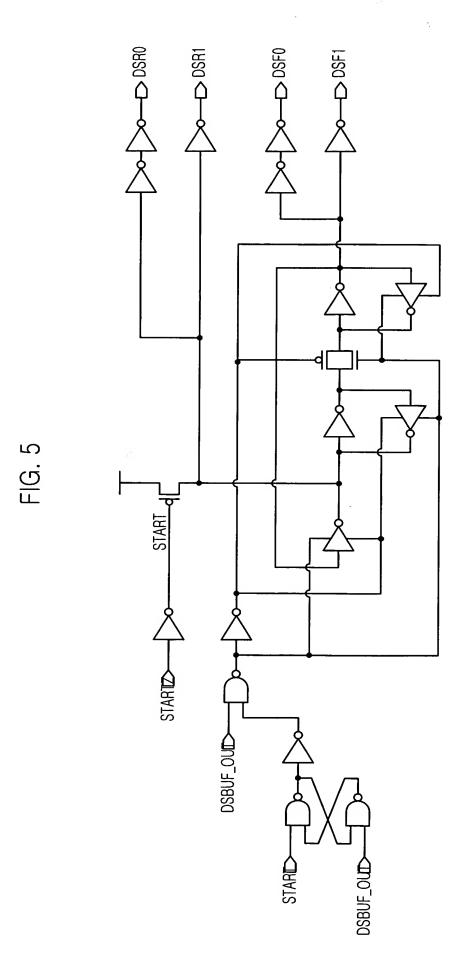
FIG. 2 (PRIOR ART)

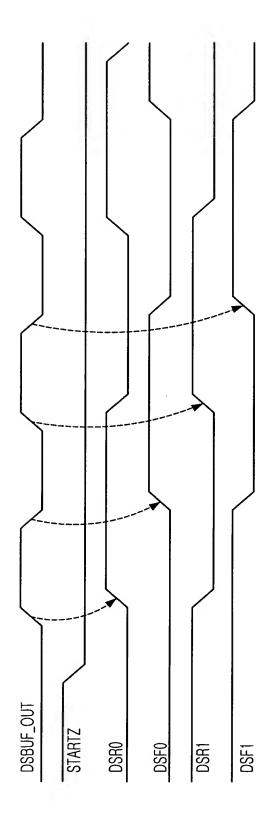


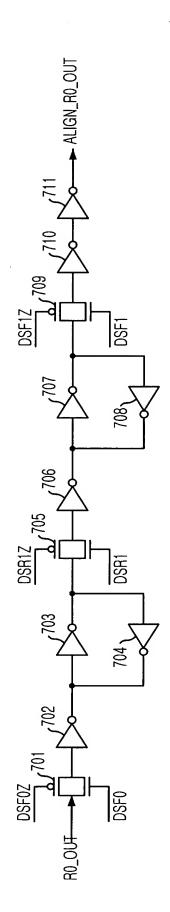












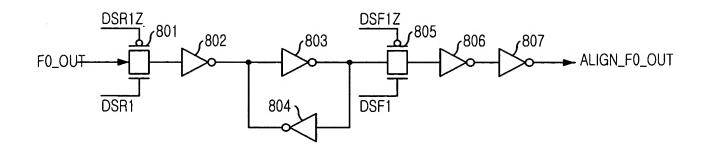


FIG. 9

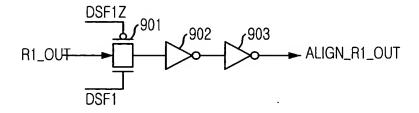


FIG. 10

